



INSTITUT
Mines-Télécom

Hardware Verification

SE303b – Conception des
systèmes sur puces (SoC)

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Outline

Introduction

Design and Verification Process

Functional Verification

Circuit Models

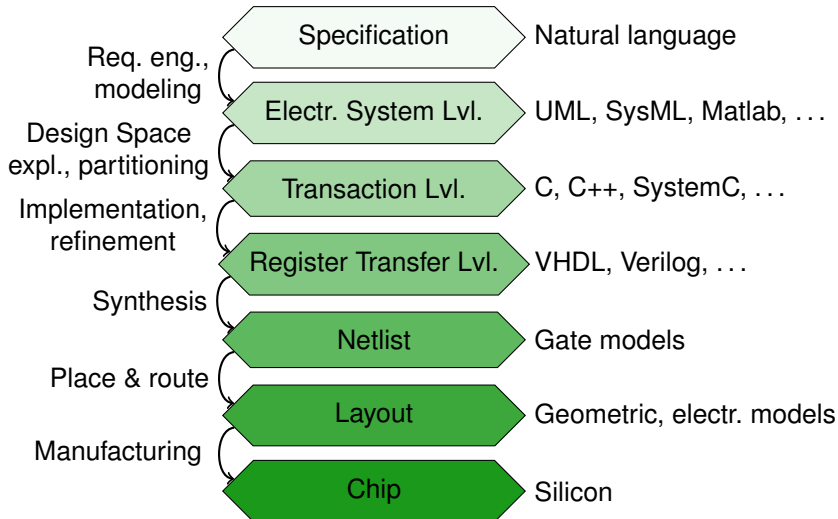
Linear Time Logic (LTL)

Computation Tree Logic (CTL)

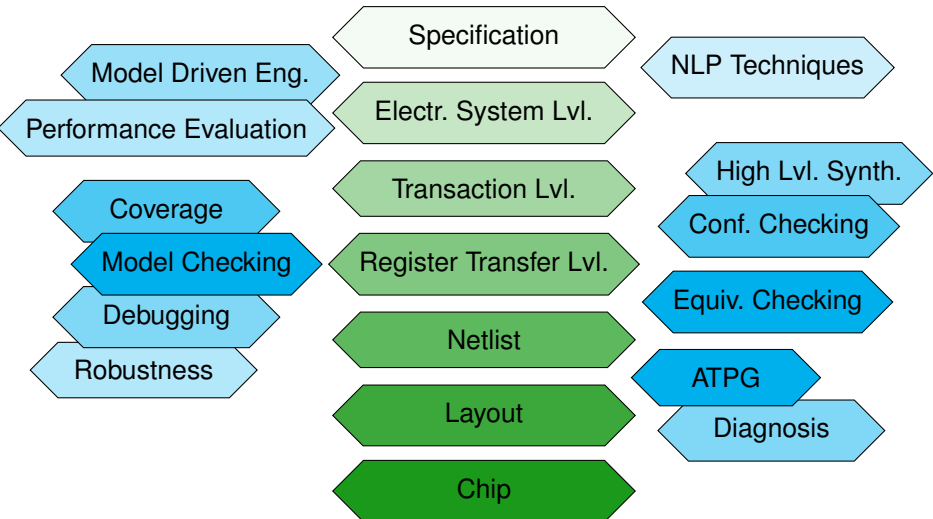
Model Checking

Hardware Test

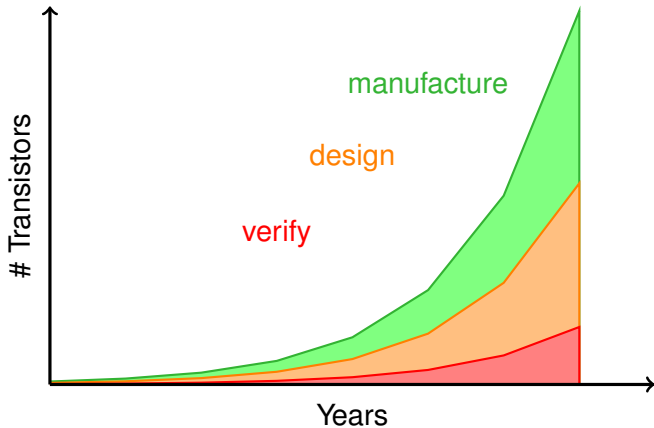
Hardware Design Flow



Hardware Verification Flow



Design Gap – Verification Gap





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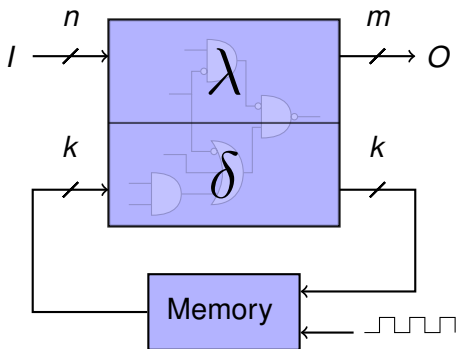
Model Checking

Hardware Test

Functional Verification

- **Dynamic verification** (= simulation)
still standard technology
- Pentium 4 overall simulated cycles < one minute
at operation speed [Bentley, 2005]
- Full coverage is **infeasible**
- Increasing use of **formal methods**

Sequential Circuit Model



Mealy Machine:

$$\mathcal{M} = (I, O, S, S_0, \delta, \lambda)$$

$$\delta : S \times I \rightarrow S$$

$$\lambda : S \times I \rightarrow O$$

$$S_0 \subseteq S$$

$$I = \{0, 1\}^n$$

$$O = \{0, 1\}^m$$

$$S = \{0, 1\}^k$$

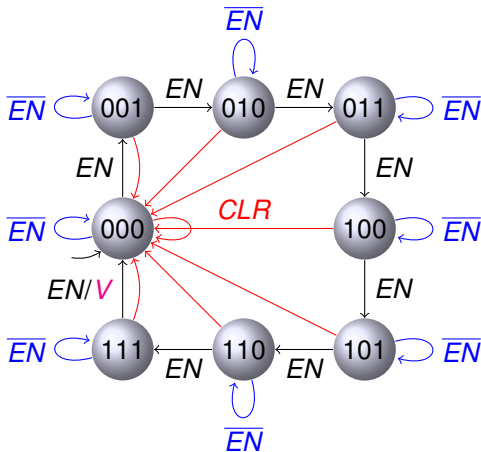
From Verilog to Mealy Machine

```
module count(CLK, EN, CLR,  
            S0, S1, S2, V);
```

```
input  CLK, EN, CLR;  
output reg S0, S1, S2;  
output  V;
```

```
assign V = S0 & S1 & S2 &  
        !CLR & EN;
```

```
always @(posedge CLK) begin  
    if (CLR)  
        {S2, S1, S0} <= 0;  
    else if (EN)  
        {S2, S1, S0}  
        <= {S2, S1, S0} + 1;  
end  
endmodule // count
```



Verification Model

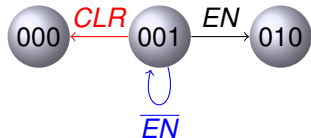
Mealy Machine:

$$\mathcal{M} = (I, O, S, S_0, \delta, \lambda)$$

$$\delta : S \times I \rightarrow S$$

$$\lambda : S \times I \rightarrow O$$

$$S_0 \subseteq S$$



Kripke Structure:

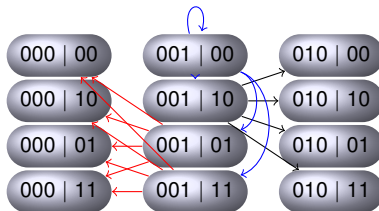
$$\mathcal{K} = (S, S_0, \delta, \mathcal{V}, \mathcal{L})$$

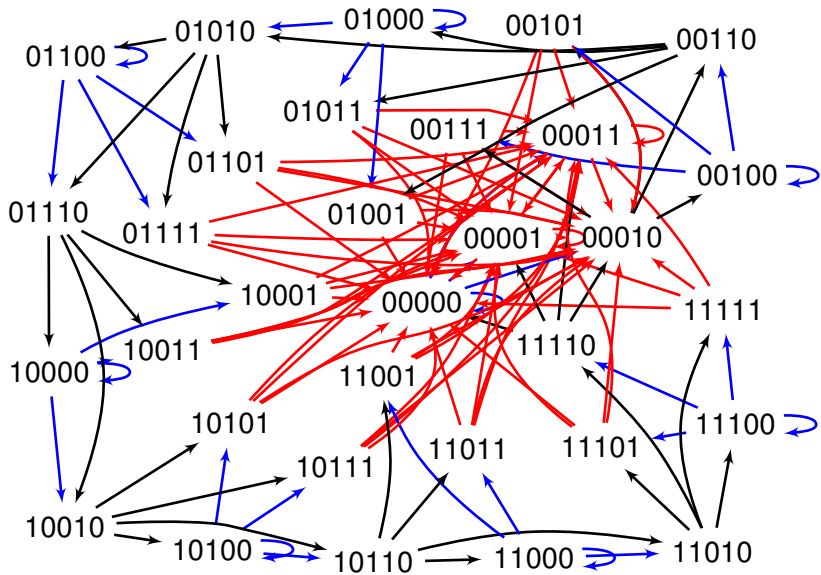
$\delta \subseteq S \times S$ transition relation

$S_0 \subseteq S$ initial states

\mathcal{V} propositional variables

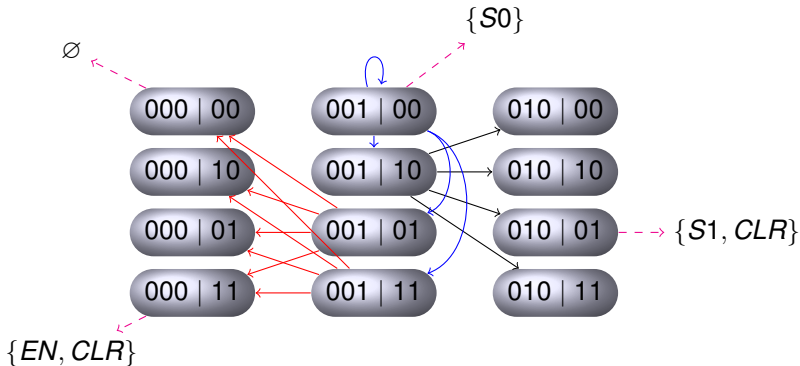
$\mathcal{L} : S \rightarrow 2^{\mathcal{V}}$ labelling function





Labelling Function

Propositional variables $\mathcal{V} = \{S2, S1, S0, EN, CLR, V\}$



What do we want to verify?

Safety

Something bad will never happen, e.g.

“The stack pointer will never overflow”

“The traffic lights will never be green at the same time”

Liveness

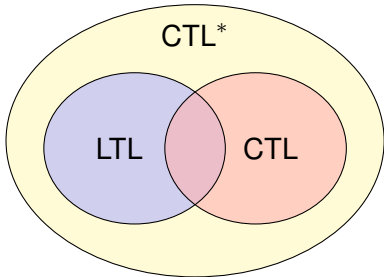
Something good will eventually happen, e.g.

“Every request will be granted”

“The cache and the main memory will eventually be consistent”

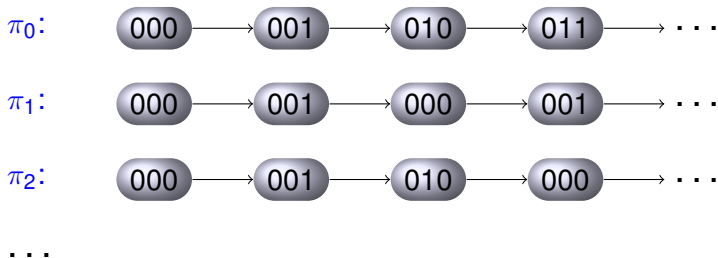
How to specify such properties?

- Temporal logic = propositional logic + time
- Discrete vs. continuous time
- Linear time view
- Branching time view

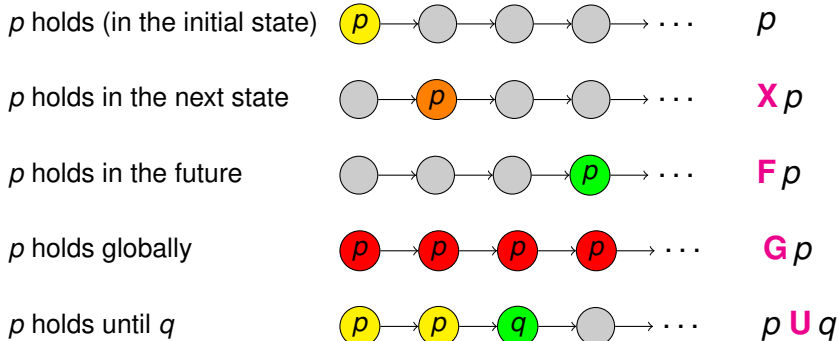


The Linear Time View

Computation paths



Linear Time Logic (LTL)



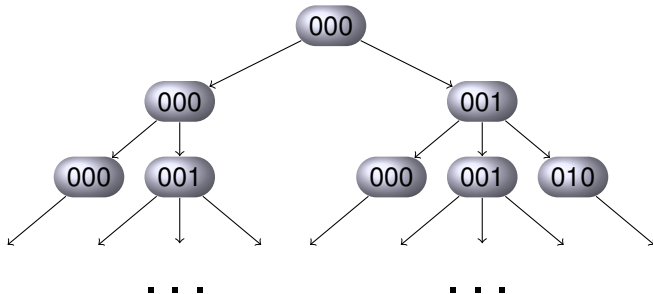
Linear Time Logic (LTL)

An LTL formula over propositional variables \mathcal{V} has the form

$$\begin{array}{l} LTL ::= p, \quad \text{where } p \in \mathcal{V} \\ | \neg \varphi \\ | \varphi \wedge \psi \\ | \mathbf{X} \varphi \\ | \mathbf{F} \varphi \\ | \mathbf{G} \varphi \\ | \varphi \mathbf{U} \psi, \quad \text{where } \varphi, \psi \in LTL. \end{array}$$

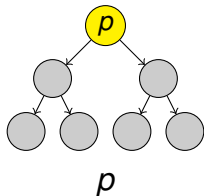
Branching Time View

Computation Tree

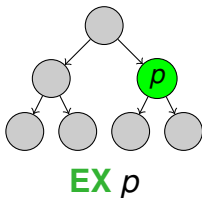


Computation Tree Logic (CTL)

Some property p holds
(in the initial state)



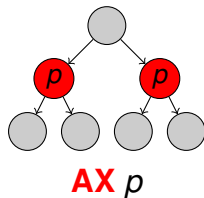
p holds in
some next state



path
quantifier

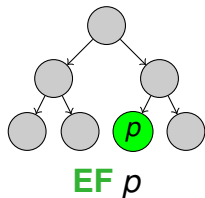
next
operator

p holds in
all next states

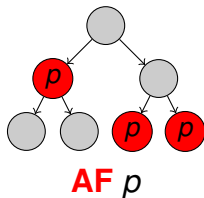


Further Modalities

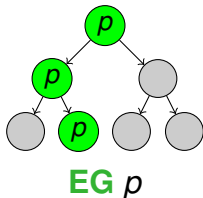
p holds in some future state



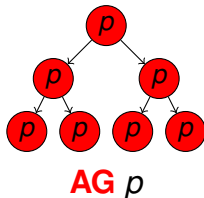
p holds eventually



p holds globally on some path

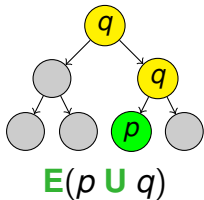


p holds globally on all paths

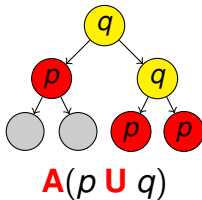


Until Modalities

On some path, q holds until p holds



On all paths, q holds until p holds



Computation Tree Logic (CTL)

A CTL formula over propositional variables \mathcal{V} has the form

$$\begin{array}{l} \text{CTL} ::= p, \text{ where } p \in \mathcal{V} \\ \quad | \varphi \wedge \psi \quad | \neg \varphi \\ \quad | \mathbf{EX} \varphi \quad | \mathbf{AX} \varphi \\ \quad | \mathbf{EF} \varphi \quad | \mathbf{AF} \varphi \\ \quad | \mathbf{EG} \varphi \quad | \mathbf{AG} \varphi \\ \quad | \mathbf{E}(\varphi \mathbf{U} \psi) \quad | \mathbf{A}(\varphi \mathbf{U} \psi), \text{ where } \varphi, \psi \in \text{CTL} \end{array}$$

What do we want to verify?

Safety

“The stack pointer will never overflow” **AG** ($sp < 4096$)

“The traffic lights will never be green at the same time” \neg **EF** ($tl_1 \wedge tl_2$)

Liveness

“Every request will be granted” **AG** ($req \rightarrow$ **AF** gnt)

“The cache and the main memory will eventually be consistent” **AF** ($mem_i = cache_i$)

Model Checking

Given a Kripke Structure \mathcal{K} and a CTL formula φ ,
check if $\mathcal{K} \models \varphi$.

How do we do this?

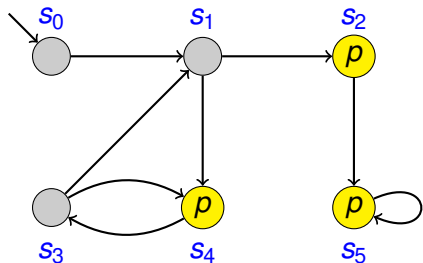
1. Compute all states in which φ holds:

$$\tau(\varphi) = \{s \in \mathcal{S} \mid \mathcal{K}, s \models \varphi\}$$

2. Check if the initial states are a subset of those states:

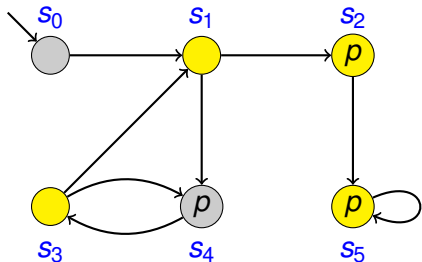
$$S_0 \setminus \tau(\varphi) = \emptyset$$

Example



$$\tau(p) = \{s_2, s_4, s_5\}$$

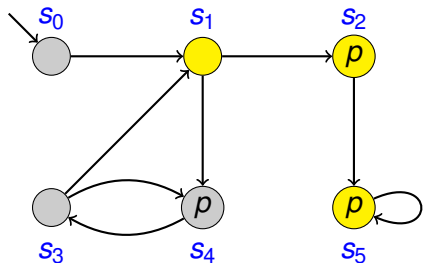
Example



$$\tau(p) = \{s_2, s_4, s_5\}$$

$$\tau(\mathbf{EX} p) = \{s_1, s_2, s_3, s_5\}$$

Example

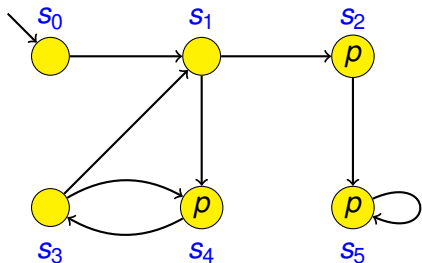


$$\tau(p) = \{s_2, s_4, s_5\}$$

$$\tau(\mathbf{EX} p) = \{s_1, s_2, s_3, s_5\}$$

$$\tau(\mathbf{AX} p) = \{s_1, s_2, s_5\}$$

Example



$$\tau(p) = \{s_2, s_4, s_5\}$$

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$$\tau(\mathbf{AX} p) = \{s_1, s_2, s_5\}$$

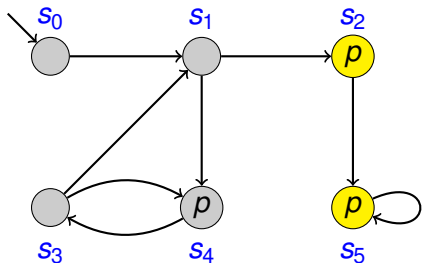
$$\tau(\mathbf{EF} p) = \{s_2, s_4, s_5\}$$

$$\cup \{s_1, s_3\} \cup \{s_0\}$$

Expansion rules:

$$\mathbf{EF} \varphi = \varphi \vee \mathbf{EX} \mathbf{EF} \varphi$$

Example



$$\tau(p) = \{s_2, s_4, s_5\}$$

$$\tau(\mathbf{EX} p) = \{s_1, s_2, s_3, s_5\}$$

$$\tau(\mathbf{AX} p) = \{s_1, s_2, s_5\}$$

$$\tau(\mathbf{EF} p) = \{s_2, s_4, s_5\} \\ \cup \{s_1, s_3\} \cup \{s_0\}$$

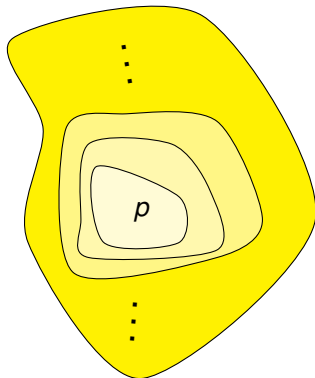
Expansion rules:

$$\mathbf{EF} \varphi = \varphi \vee \mathbf{EX} \mathbf{EF} \varphi$$

$$\mathbf{AG} \varphi = \varphi \wedge \mathbf{AX} \mathbf{AG} \varphi$$

$$\tau(\mathbf{AG} p) = \{s_2, s_4, s_5\} \cap \{s_2, s_5\}$$

Fixed Point Algorithm for EF p



$$S_0 = p$$

$$S_1 = p \cup \mathbf{EX} p$$

$$S_2 = p \cup \mathbf{EX} p \cup \mathbf{EX} \mathbf{EX} p$$

\dots

$$S_n = p \cup \bigcup_{i=1}^n \mathbf{EX}^i p = S_{n-1}$$

$$\Rightarrow S_n = \tau(\mathbf{EF} p)$$

Fixed Points

Let $f : \mathcal{P}(S) \rightarrow \mathcal{P}(S)$ a set-valued function and $Z \subseteq G$.

- Z is called a **fixed point** of f if $f(Z) = Z$
- Z is the **least fixed point** of f if it is a fixed point and for all other fixed points U of f it holds that $Z \subseteq U$.
- Z is the **greatest fixed point** of f if it is a fixed point and for all other fixed points U of f it holds that $U \subseteq Z$.

Fixed Points (2)

A function $f : \mathcal{P}(S) \rightarrow \mathcal{P}(S)$ is called **monotone** if for all $X, Y \subseteq S$

$$X \subseteq Y \Rightarrow f(X) \subseteq f(Y) \quad (1)$$

Knaster-Tarski Theorem

Let $f : \mathcal{P}(S) \rightarrow \mathcal{P}(S)$ be a monotone function. Then f has a least and a greatest fixed point.

- $\bigcup_{n \geq 1} f^n(\emptyset)$ is the least fixed point of f .
- $\bigcap_{n \geq 1} f^n(S)$ is the greatest fixed point of f .

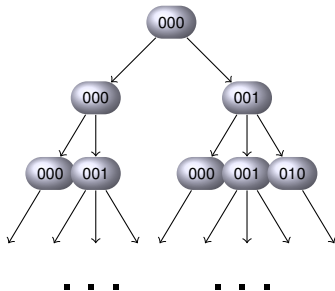
CTL Model Checking

Let $\mathcal{K} = (\mathcal{S}, \mathcal{S}_0, \delta, \mathcal{V}, \mathcal{L})$ be a Kripke structure.

$$\begin{aligned}\tau(p) &= \{s \in \mathcal{S} \mid p \in \mathcal{L}(s)\} \\ \tau(\varphi \wedge \psi) &= \tau(\varphi) \cap \tau(\psi) \\ \tau(\varphi \vee \psi) &= \tau(\varphi) \cup \tau(\psi) \\ \tau(\neg\varphi) &= \mathcal{S} \setminus \tau(\varphi) \\ \tau(\mathbf{EF} \varphi) &= \mathbf{lfp}Z. \tau(\varphi) \cup \mathbf{EX}(Z) \\ \tau(\mathbf{AF} \varphi) &= \mathbf{lfp}Z. \tau(\varphi) \cup \mathbf{AX}(Z) \\ \tau(\mathbf{EG} \varphi) &= \mathbf{gfp}Z. \tau(\varphi) \cap \mathbf{EX}(Z) \\ \tau(\mathbf{AG} \varphi) &= \mathbf{gfp}Z. \tau(\varphi) \cap \mathbf{AX}(Z) \\ \tau(\mathbf{E}(\varphi \mathbf{U} \psi)) &= \mathbf{lfp}Z. \tau(\psi) \cup (\tau(\varphi) \cap \mathbf{EX}(Z)) \\ \tau(\mathbf{A}(\varphi \mathbf{U} \psi)) &= \mathbf{lfp}Z. \tau(\psi) \cup (\tau(\varphi) \cap \mathbf{AX}(Z))\end{aligned}$$

Model Checking

- Complexity depends heavily on state space
- Need for efficient data structures
- **State space explosion** still a problem
- Works for small to medium (or very regular) systems
- Popular tool: NuSMV
[Cimatti et al., 2002]
- Ongoing research





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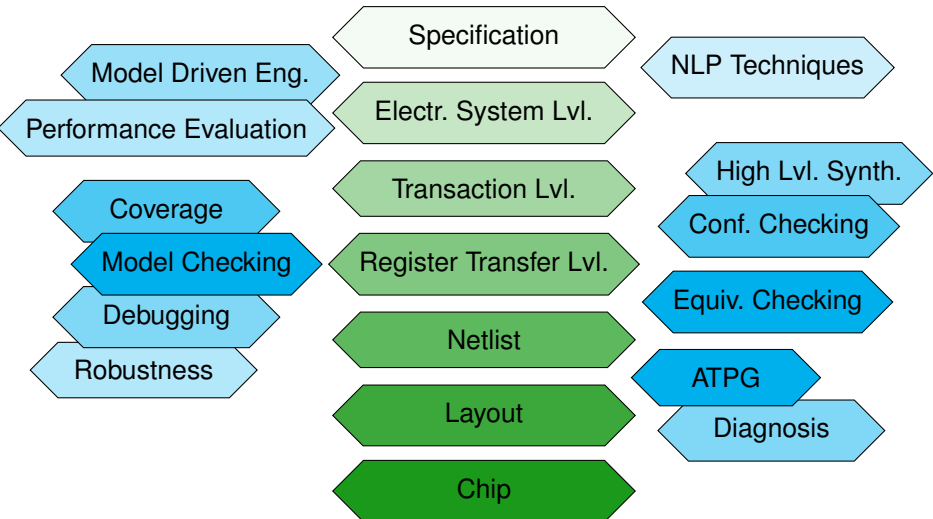
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Hardware Verification vs Test

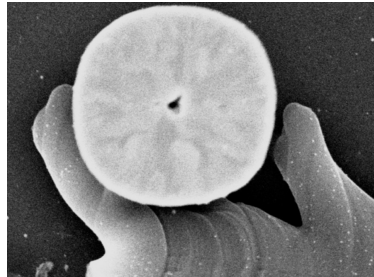
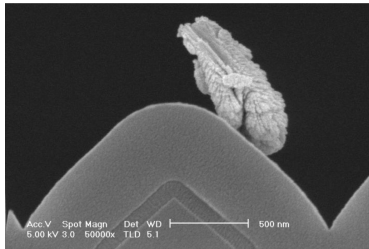
Verification

- Detect **design bugs**
- Extract properties from **requirements**
- Applied on **RTL code**
- High **manual** effort

Test

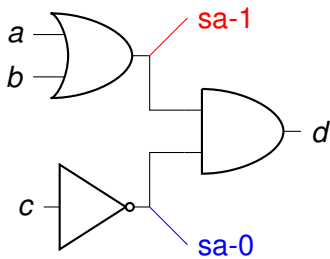
- Detect **physical defects**
- Test generation from **netlist** according to **fault model**
- Applied on **fabricated chips**
- High **automation**

Physical Defects



[Source: IEEE Spectrum “The Art of Failure”]

Stuck-at Fault Model



a	b	c	d
0	0	0	00
0	0	0/1	
0	0	1	0
0	1	0	11/0
0	1	1	0
1	0	0	11/0
1	0	1	0
1	1	0	11/0
1	1	1	0

- $\langle 000 \rangle$ is a test vector for the shown stuck-at-1 fault
- $\{\langle 010 \rangle, \langle 100 \rangle, \langle 110 \rangle\}$ are test vectors for the stuck-at-0 fault

Automatic Test Pattern Generation

ATPG

- Create a list of all possible (stuck-at) faults
- For each fault:
 - Find a test pattern
 - Drop all other faults detected by this pattern
- Untestable faults?
- Hard to test faults?
- Sequential tests?
- Test compression?

References I



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Validating a modern microprocessor.

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Cimatti, A., Clarke, E., Giunchiglia, E., Giunchiglia, F., Pistore, M., Roveri, M., Sebastiani, R., and Tacchella, A. (2002).

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