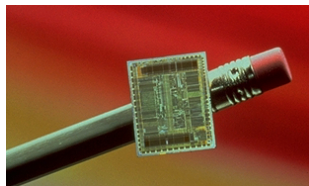


TELECOM  
ParisTech



INSTITUT  
Mines-Télécom



# ICS904/EN2 : Design of Digital Integrated Circuits

L2 : Structural design of digital circuits  
(1/2))

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PARIS-SACLAY



# Outline

Introduction

MOS complementary logic (CMOS)

Pass Transistor Logic

# Integrated logic

- How to build logic functions with electronic components ?
- Many possible implementations . . .
  - derived from the manipulation of logical expressions.
  - derived from component properties (MOS transistors, bipolar . . .)
- Arbitrary choice of a physical variable to represent the logic states
- Many paths explored in the years 70-90
- Major classes of solutions stabilized since.
- But research still continues . . .

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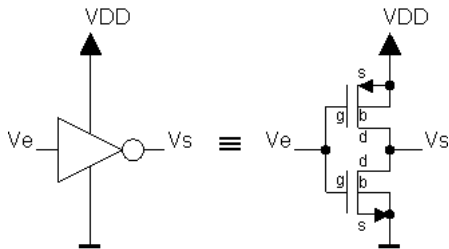
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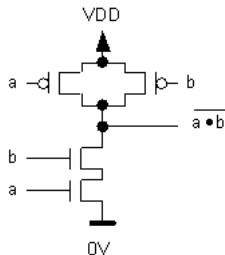
Pass Transistor Logic

## CMOS inverter

- The selected supply voltage is the reference for defining the Boolean signal
- Harnessing the symmetrical behavior of NMOS and PMOS transistors.



# The 2 input NAND gate



a	b	Output
0	0	1
0	1	1
1	0	1
1	1	0

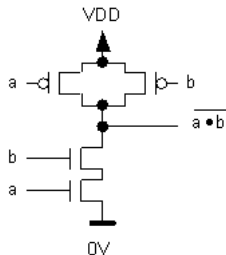
## NMOS network

- ON if the two NMOS transistors are "ON"
- OFF if one of the two NMOS transistors is "OFF"

## PMOS network

- ON if one of the two PMOS transistors is "ON"
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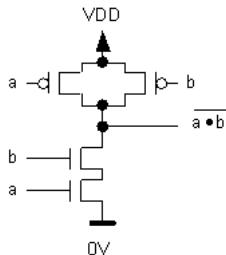
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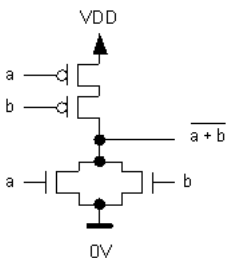
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# The two input NOR gate



a	b	Output
0	0	1
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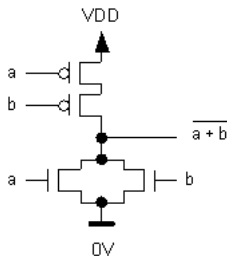
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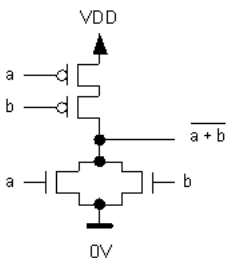
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# CMOS logic

## Generalization to other boolean functions

- Given the truth-table of boolean function.
- PMOS networks are used for the logic ones of the boolean function.
- NMOS networks are used for the logic zeros of the boolean function.
- A one to one NMOS/PMOS structure
- Implementable gates have a function of the form
$$F(x_0, x_1, \dots, x_n) = \overline{\sum \prod x_i}$$
- Other boolean functions are assemblies of these primitive gates.

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Construction methods for functions of the form  $F = \sum \overline{\prod x_i}$

## ■ First, build the NMOS network :

- Express the  $\overline{F(x_0, x_1, \dots, x_n)}$  function in the form  $\sum \prod x_i$
- Perform any factorisation/simplification.
- Remaining  $\prod$  match with series of NMOS transistors (or network of NMOS transistors).
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Construction methods for functions of the form  $F = \sum \overline{\Pi x_i}$

- Two remarks :
  - Simplest CMOS gates are inverting gates (NAND is smaller than AND)
  - Dual PMOS and NMOS networks may be used :
    - Use parallel PMOS network when series of NMOS networks are used
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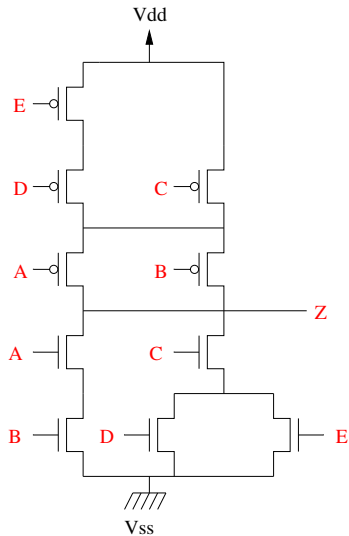
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$$Z = \overline{A \cdot B + C \cdot (D + E)}$$



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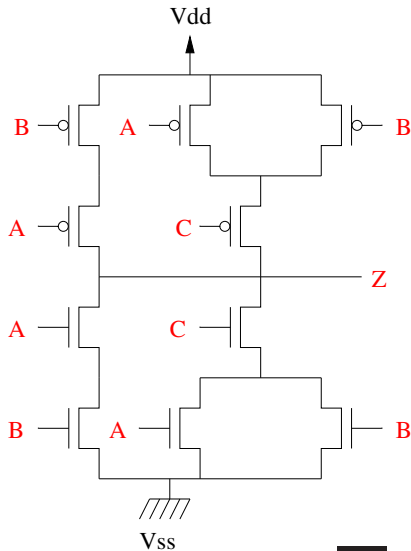
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- Q1 : Build the gate using optimum optimisation methods
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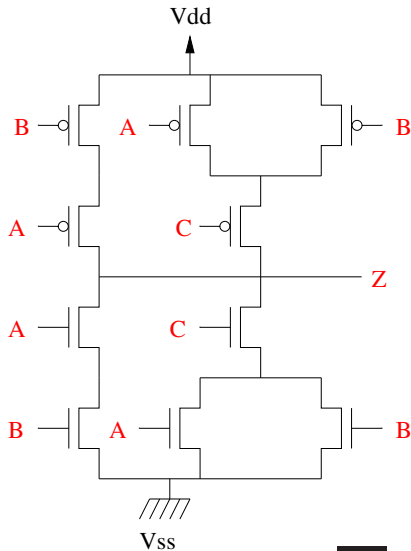
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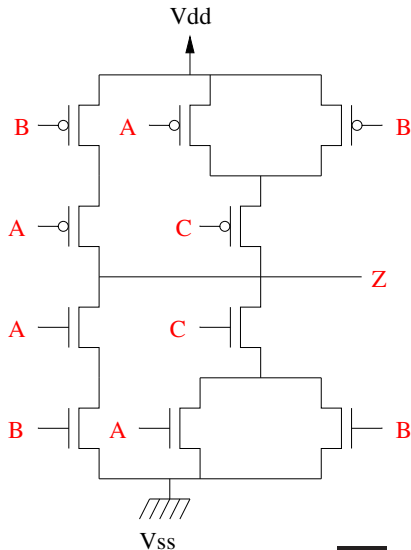
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## Low/High input counts

- Series of transistors : the body effect (see lecture L1) leads to slow high  $V_t$  transistors.
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  - AND6 gate example, 28nm process, 1v supply voltage, all NMOS transistors of equal size,  $w_p/w_n = 1.6$ , no output load.
  - Test cases : (1) All inputs change, (2) One input changes.
  - Q1 : Setup a simple model of propagation type, using resistive approximation
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|--------------------|--------------------|--------------------|
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# CMOS logic

## non complementary PMOS/NMOS networks

- NMOS and PMOS networks may be simultaneously OFF.
- Usage : Input/Output trceivers for external busses.
- Tristate inverter.

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0	1	highZ
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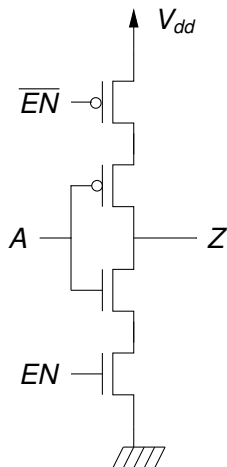
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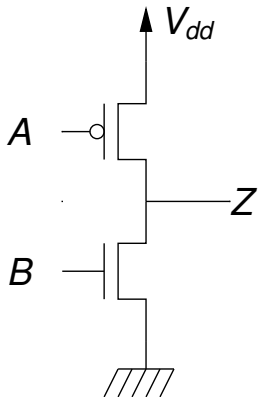
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# Outline

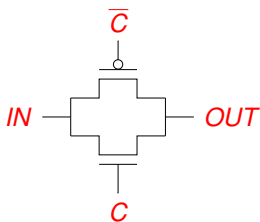
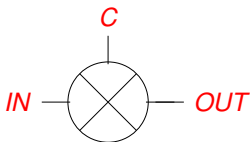
Introduction

MOS complementary logic (CMOS)

Pass Transistor Logic

# Pass Transistor Logic

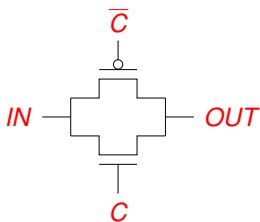
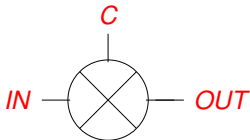
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- Warning : Passive circuit, no signal regeneration along the path "IN" to "OUT"

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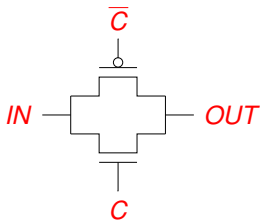
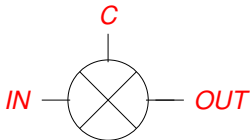


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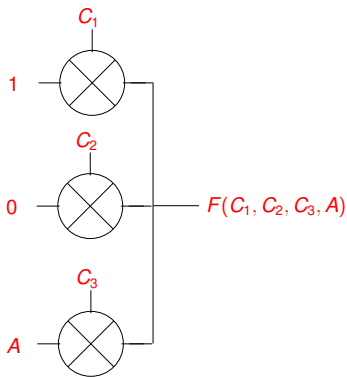
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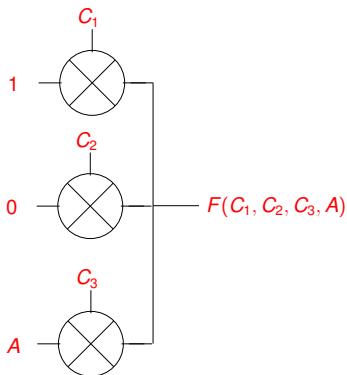
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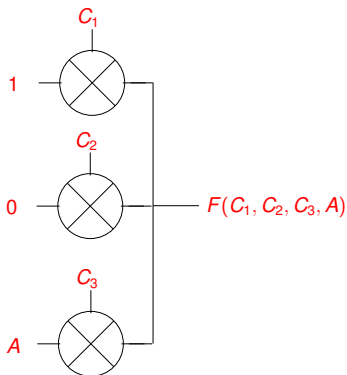
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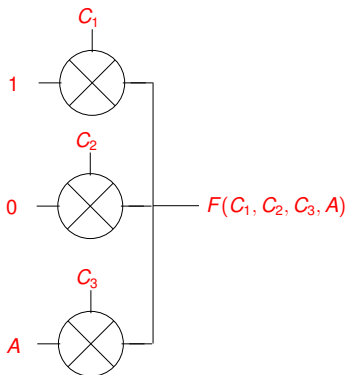
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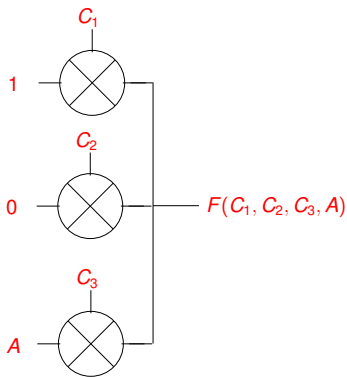
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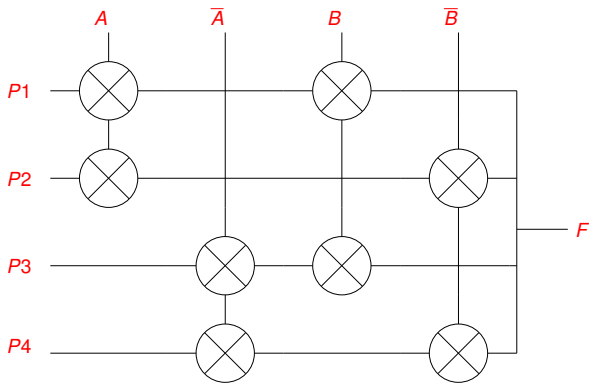
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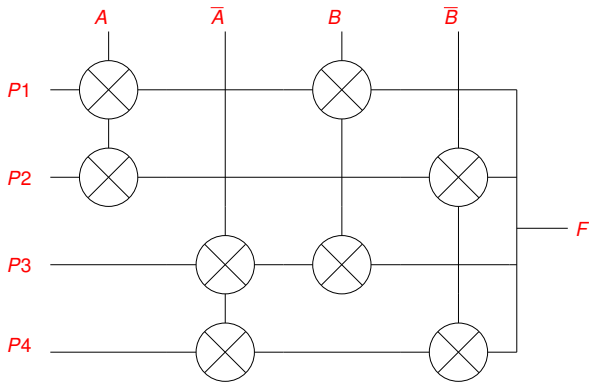


■  $F = P_1 \cdot A \cdot B + P_2 \cdot A \cdot \bar{B} + P_3 \cdot \bar{A} \cdot B + P_4 \cdot \bar{A} \cdot \bar{B}$

- Division of the truth table into four sub-tables (P1,P2,P3,P4) based on the full decoding of the 2 inputs A and B.

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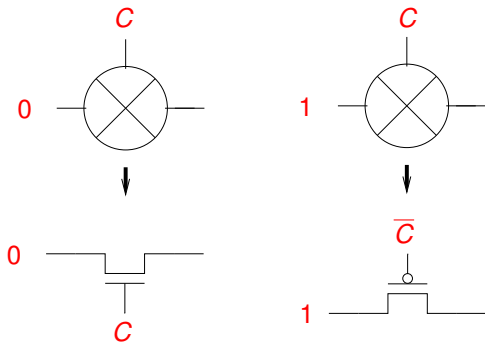
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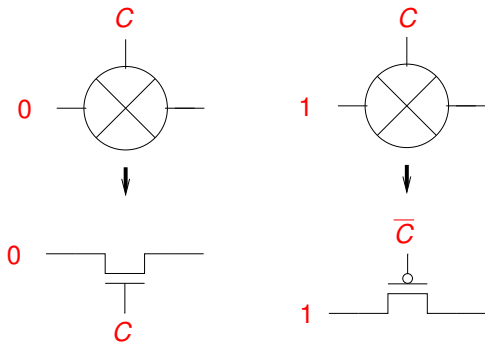
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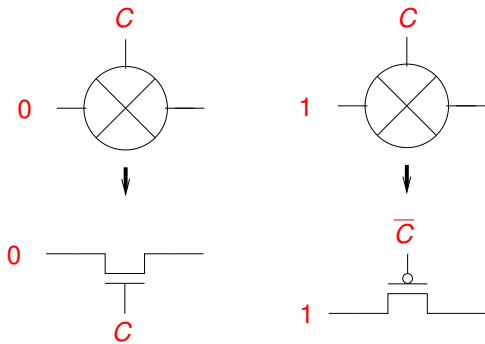
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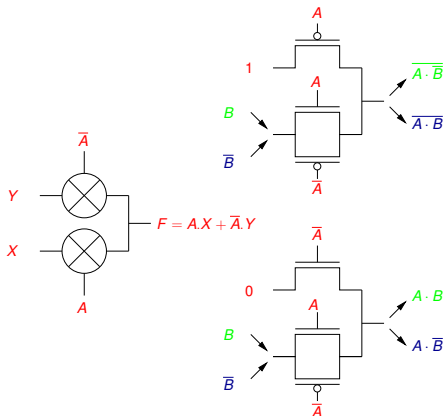
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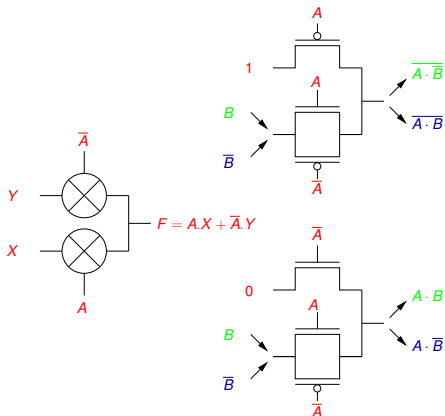
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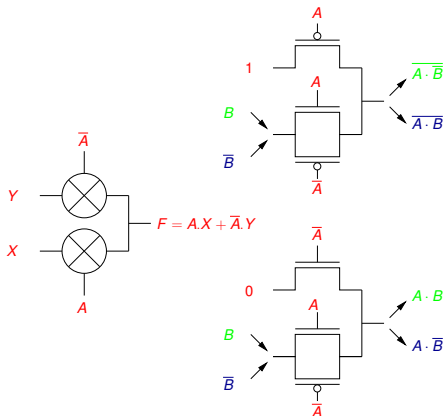
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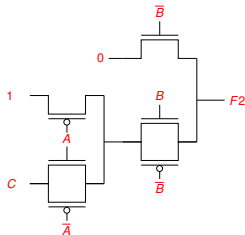
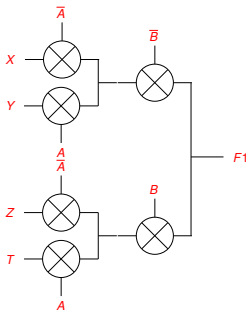
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## Trees of muxes



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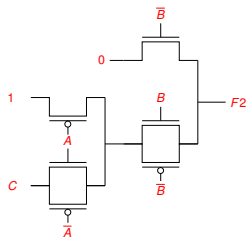
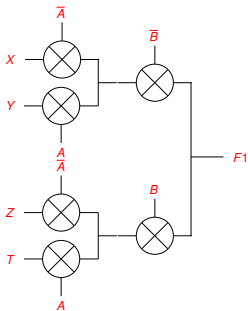
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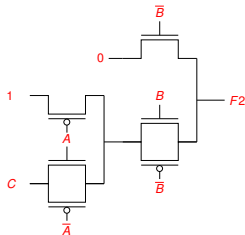
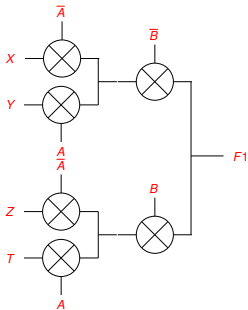
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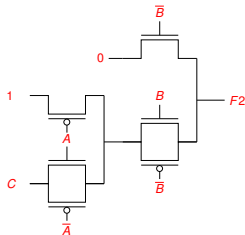
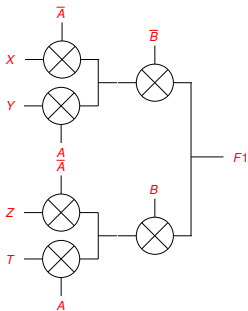
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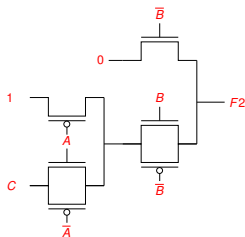
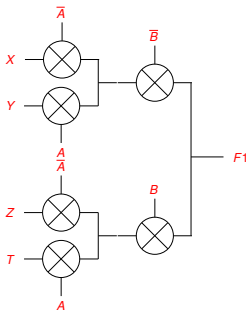
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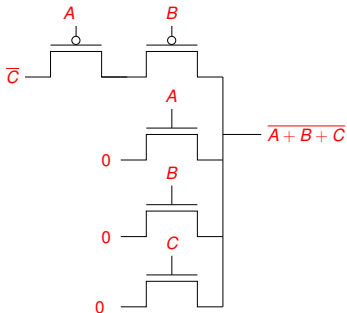
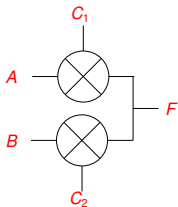
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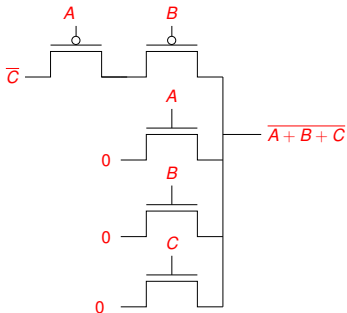
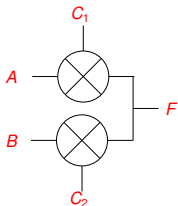
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- Several branches may be simultaneously ON.
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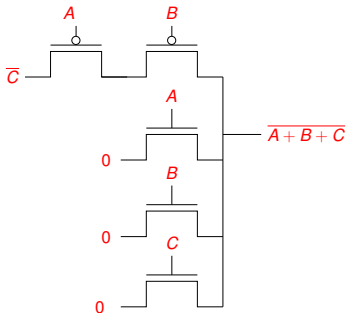
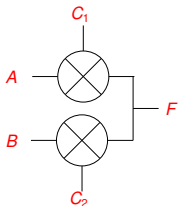
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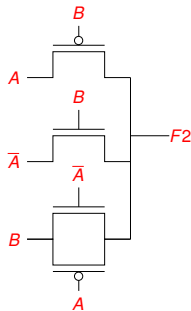
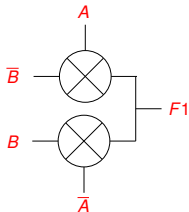
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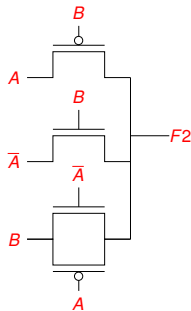
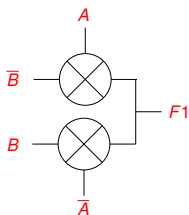
## Two inputs XOR gate



- XOR :  $A \cdot \bar{B} + \bar{A} \cdot B$
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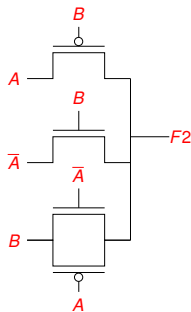
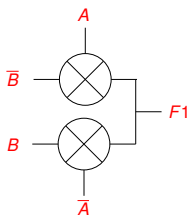


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## Chains of pass transistor logic / versus chain of invertors

- Passive propagation.
- RC time accumulation
- Test condition : CMOS 28nm,  $V_{DD} = 1V$ .
- Test case 1 : 2 invertors separated by N pass gates.
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N	1	2	3	4	5	6	7
Tp pass chain (ps)	7	11	17	24	32	42	53
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## Examples

- **Q1** : Design of a 2 inputs XOR gate
  - **Q1.1** : How many transistors in CMOS logic.
  - **Q1.2** : Compare with pass transistor logic.
- **Q2** : Ripple carry adder.
  - **Q2.1** : Design the boolean function computing the output carry of a "Full adder" using CMOS logic.
  - **Q2.2** : Optimize the carry propagation of a 2N-bits ripple carry adder.
  - In a full-adder, the output carry may be calculated as follows :
    - $C_{OUT} = G + P \cdot C_{IN}$
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- Requires less transistors than CMOS logic . . .
- Partially passive logic. . .
  - Requires buffers every 2 to 4 paths. . .
  - Performances of a gate alone are difficult to assess :  
Performance evaluation at the assembly level. . . .
- Gate inputs are not only transistor Gates but also transistor Drains or Sources.
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