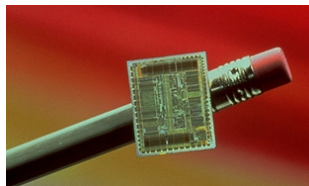


TELECOM
ParisTech



INSTITUT
Mines-Télécom

université
PARIS-SACLAY



ICS904/EN2 : Design of Digital Integrated Circuits

L3 : Structural design of digital
circuits(2/2)

Yves MATHIEU

yves.mathieu@telecom-paristech.fr



Outline

Dynamic logic

Differential logic

Application specific logic

Performance optimization

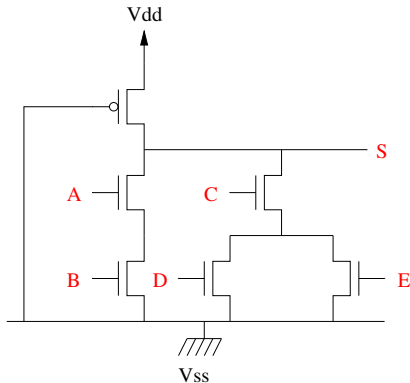
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Practical work

From NMOS logic to dynamic logic

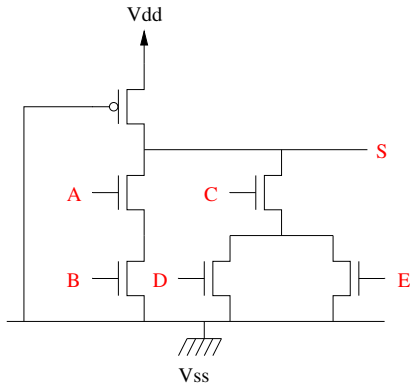
pseudo-NMOS logic



- Replacement of the PMOS network by a passive load.
- Smaller : The "1" values of the truth table are implicit values.
- CONFLICT : When NMOS network is ON : steady-state current.

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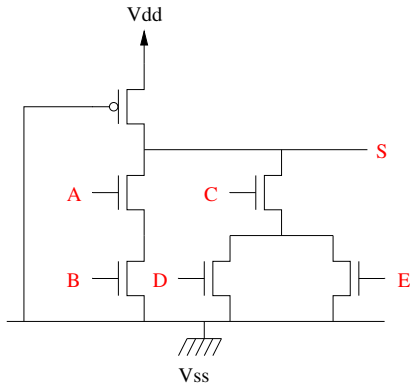
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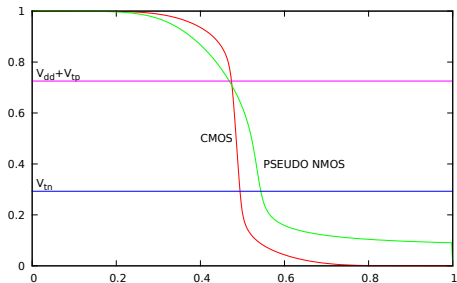
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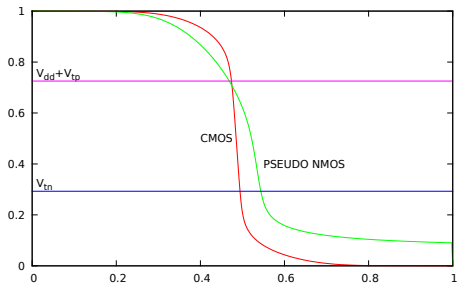
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■ How to avoid a choice between speed and low-power/robustness.

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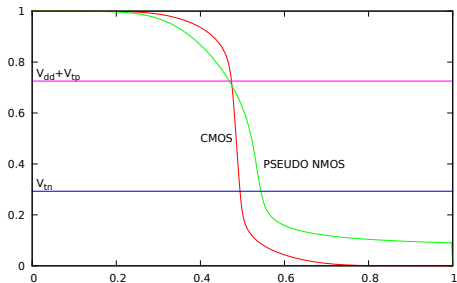
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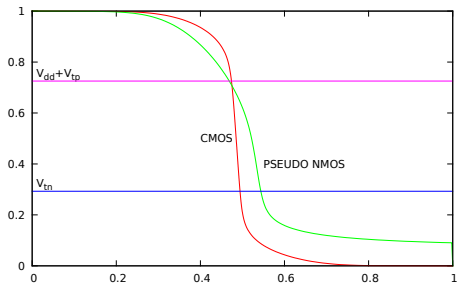
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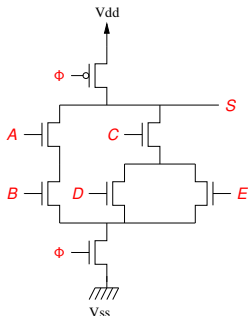
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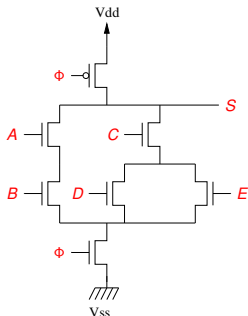
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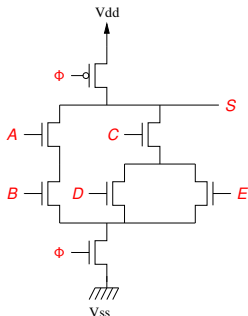
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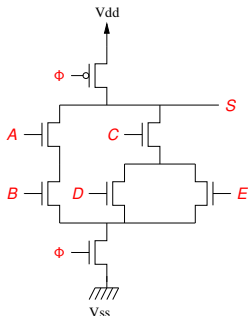
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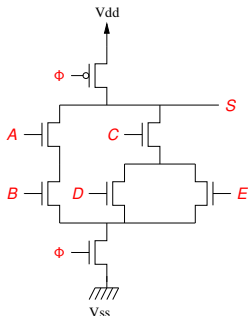
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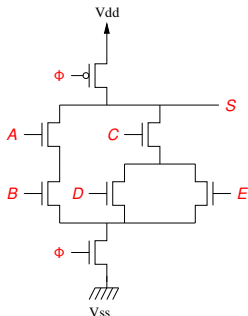
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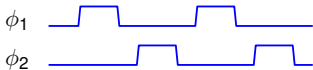
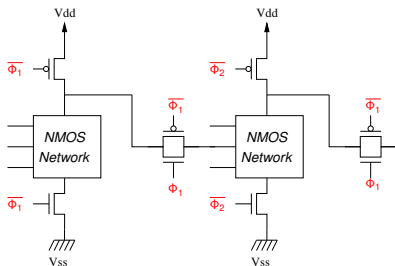
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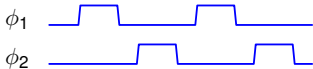
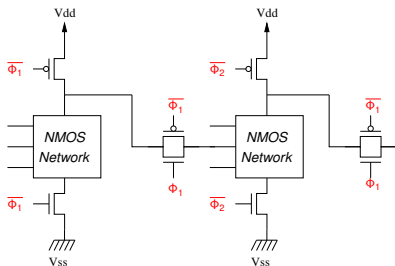
Two phases dynamic logic



- Two clocks with non overlapping phases.
- Cell isolation using pass transistor logic and acting as a register.
- Fully cascadable, but odd and even cells should alternate
- Deep pipelining (no more than one gate level between each pipeline register)

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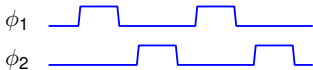
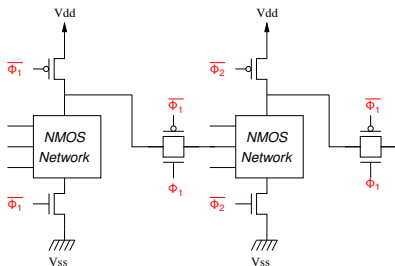
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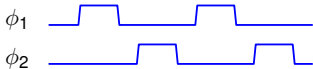
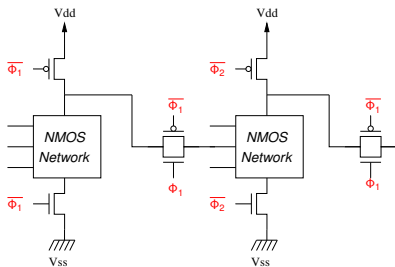
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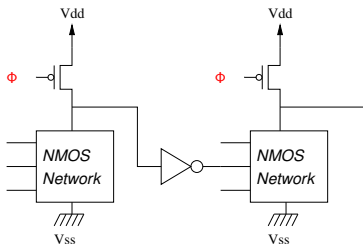


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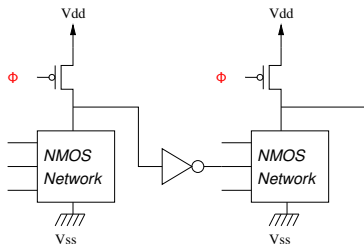
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- Warning : only non-inverting gate can be implemented

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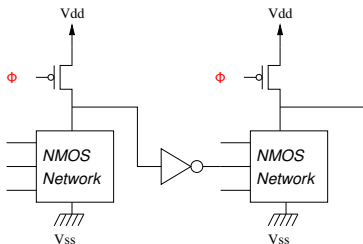
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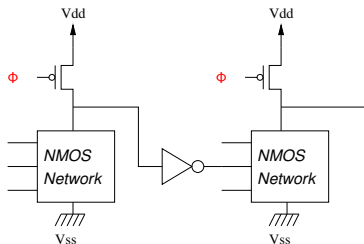
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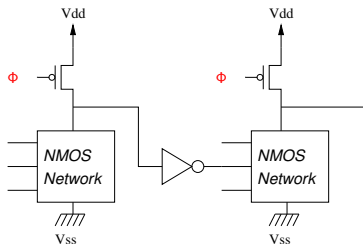


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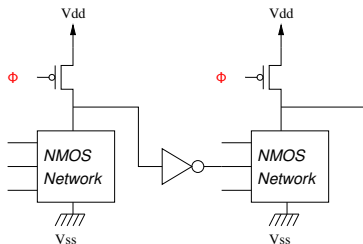


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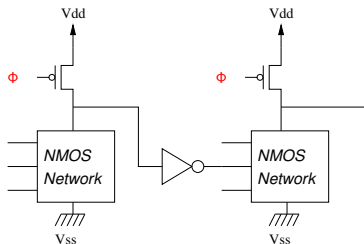


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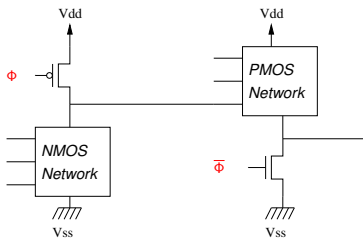


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Dynamic logic

Domino N-P logic



- Simplified : no more inverter
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- Warning : NMOS gates should alternate with PMOS gates...



Dynamic logic

Summary

- Very high speed logic (very small capacitive loads)
- Very often used during 80-90 years
- Example : High speed carry chain for arithmetic computation in microprocessors
- But : Clock is loaded by all cells... (power consumption of the clock network)
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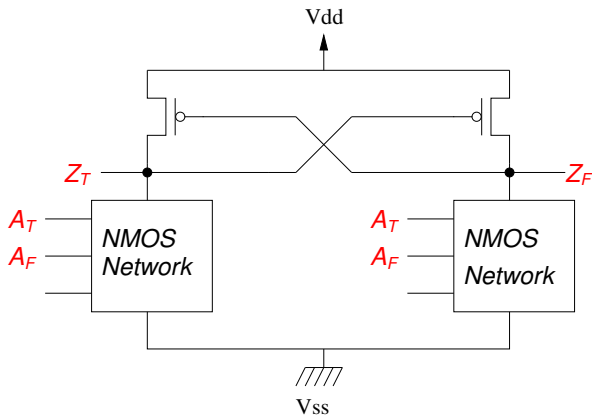
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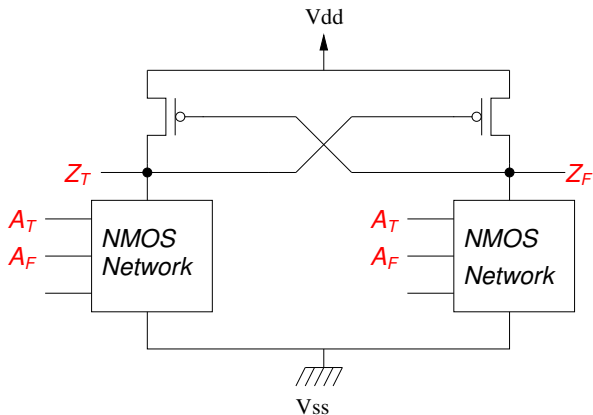
Cascode Voltage Switch Logic



- Warning : conflicts during output transitions.
- Slower than CMOS logic.
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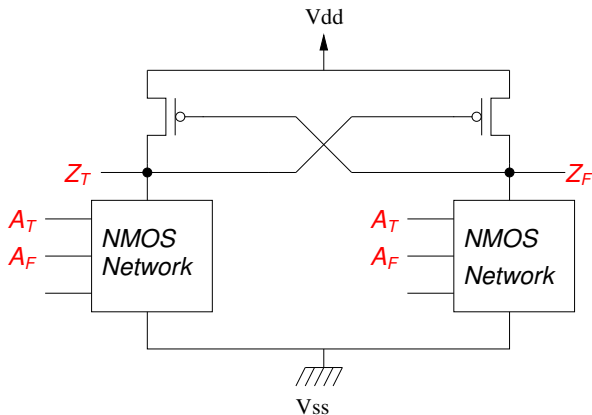
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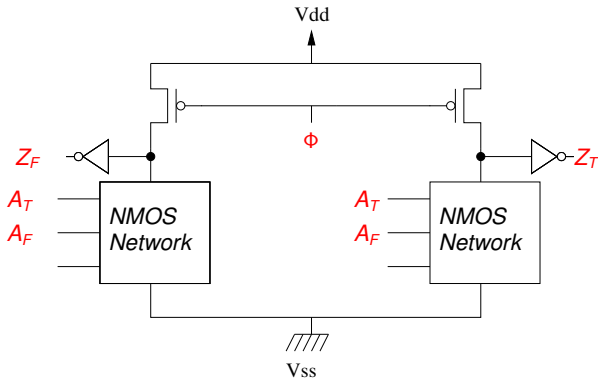
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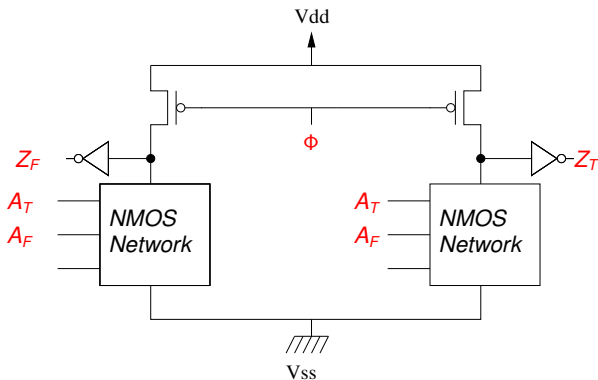
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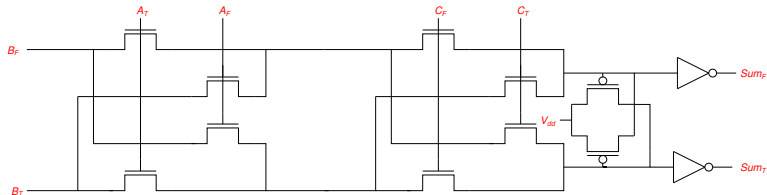
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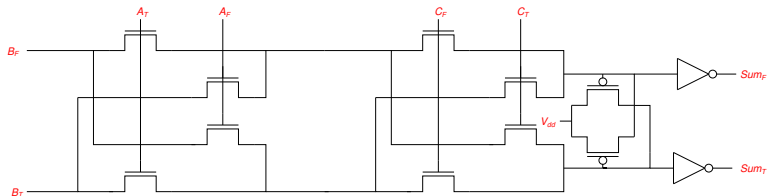
CPL : Complementary Pass Logic



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- Using *low* V_t transistor for the network, and *high* V_t transistors for the invertors helps speed optimization
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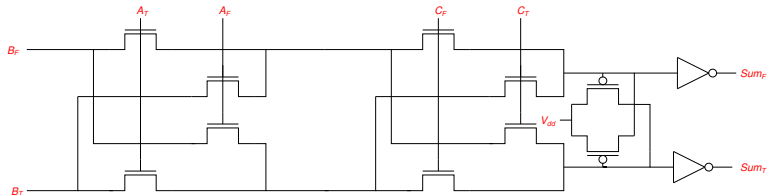
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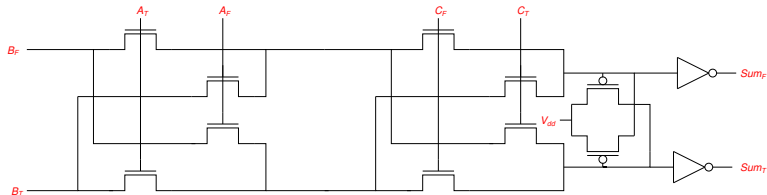
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Differential logic

Application specific logic styles

- Current Mode Logics
- Adiabatic Logic
- SubTreshold Logic
- ...



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Outline

Dynamic logic

Differential logic

Application specific logic

Performance optimization

Sequential cells

Standard cell design

Practical work



Performance metrics

Introduction

- Area of the logic gates.
- Speed of the logic gates.
- Power consumption of the logic gates
- Noise margin of the logic gates
- EDP : "Energy Delay Product" of the logic gates.
- Near threshold or Sub-threshold behavior.
- Robustness of the design.
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Buffer optimization example

simple inverter

- Problem definition : What is the fastest way to transmit a data from the input of gate A, to the inputs of gates connected to A ?
- The timing model of gate A is known : $T_{pA} = T_{p0A} + R_A \cdot C_{load}$
- The inputs of the gates connected to A are modeled by a load capacitor C_{LdA}
- A parametrized inverter can be used :
 - $T_{pIV}(\alpha) = T_{p0IV} + (R_{0IV}/\alpha) \cdot C_{load}$
 - $C_{InIV}(\alpha) = C_{0InIV} \cdot \alpha$
 - with $\alpha \geq 1.0$
- The inverter is inserted between gate A and the other gates.
- Compute the propagation time through the gates α
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several invertors

- The inverter is replaced by two successive invertors with parameters α_0 and α_1 .
- What are the optimal sizes of α_0 and α_1 for a minimum propagation time ?
- Compute the value of the minimum propagation time.
- The two invertors are replaced by N successive invertors with parameters $\alpha_0 \dots \alpha_{N-1}$.
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Buffer optimization example

How to transmit a data on a long wire

- The long wire as a distributed RC model.
- Distributed invertors along the line may help minimizing overall propagation time.
- Same kind of optimization but with a non linear model of the propagation time through the line



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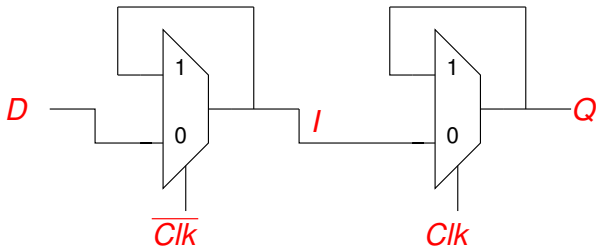
Sequential cells

Standard cell design

Practical work

positive edge-triggered D flip-flop

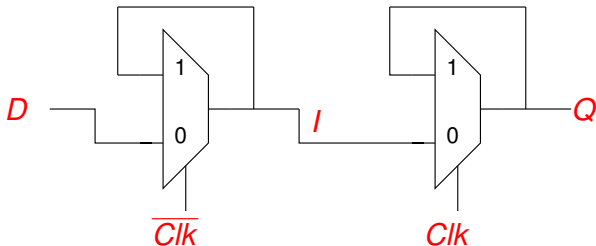
Theoretical Master/Slave flip-flop



- Muxes with loops define 2 storage elements (Master and Slave)
- Master (resp. Slave) holds its value while Slave (resp. Master) is transparent.
- Skew between the two clocks should be avoided (race condition).
- D signal should respect timing conditions.
 - Setup time / Hold time

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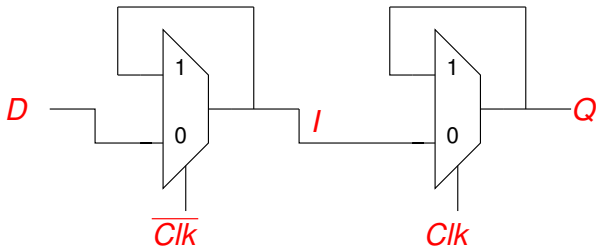
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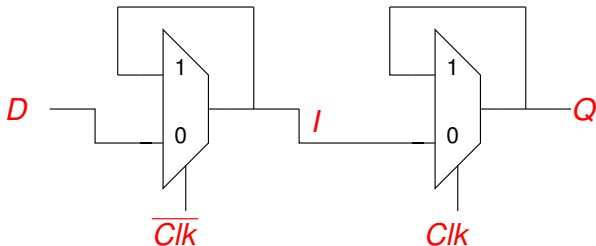
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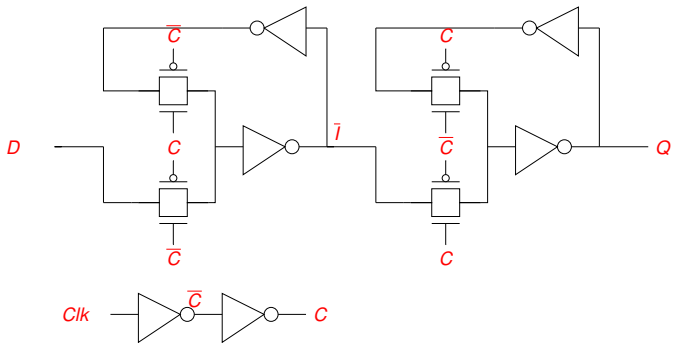
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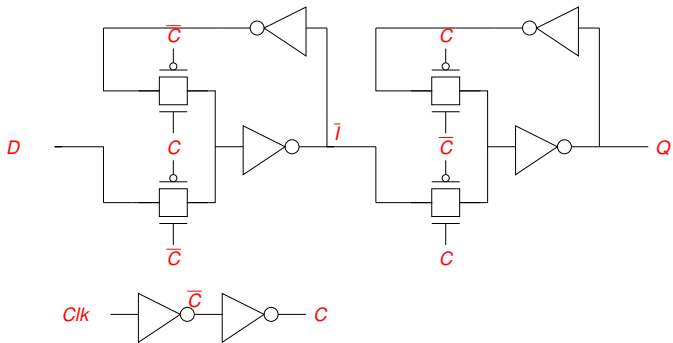
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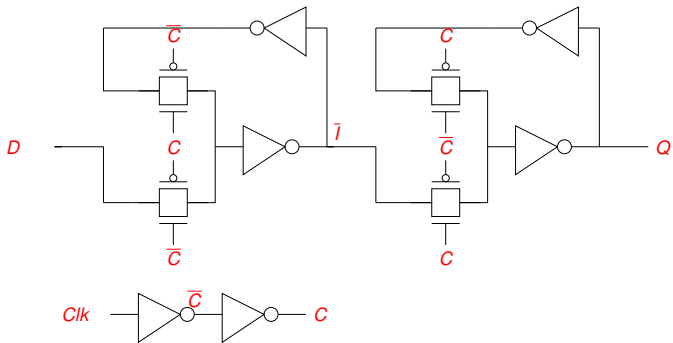
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- Warning D input is on the Drain of a transistor
- One can mix CMOS logic and pass transistor logic (using tristate inverters).
- $Q1$: Design a D flip/flop using tristate inverters

practical design



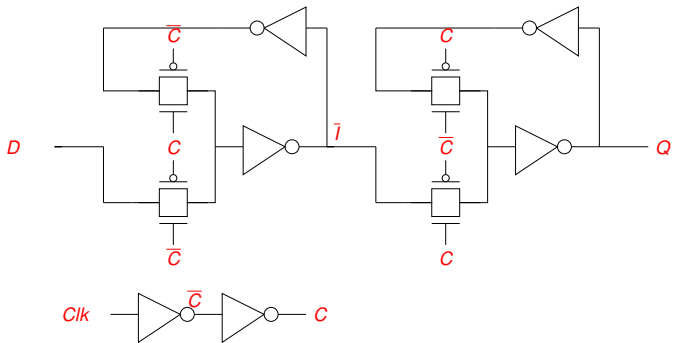
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"Standard Cells" versus "Full Custom"

Full Custom

- Manual layout of all needed cells.
- Long elec. simulations for verif. of a whole block.
- Wide logic styles choice.
- Scripting may help layout phases.
- Ultimate optimisation for speed power or area.
- Only for high value added digital or analog blocs.

Standard Cells

- Layout design limited to generic cells.
- Electrical simulation for cell properties extraction.
- Small logic styles choice.
- Automation of synthesis, place and route phases.
- Suboptimal for speed power and area.
- When time-to-market is the main criterion.

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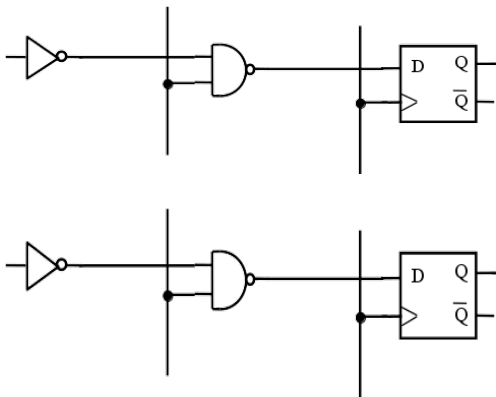
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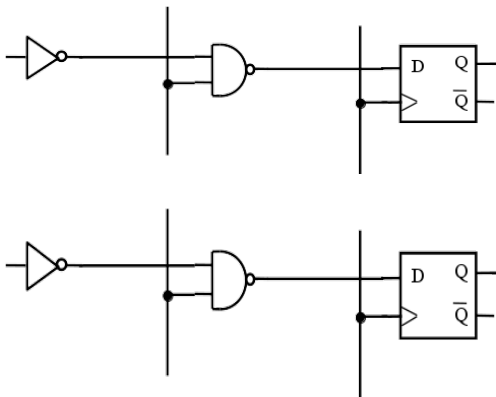
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Standard cell principles



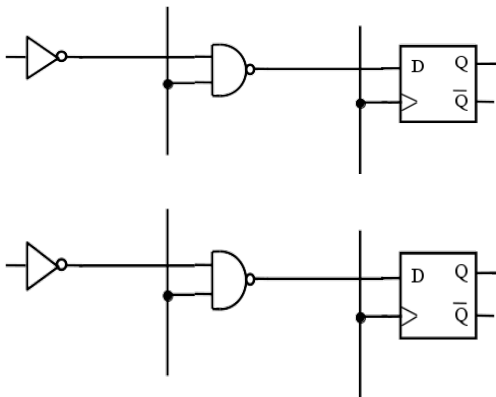
- All cells have same height
- Power supply and Ground connected by abutment.
- Cell design should be free of DRC error.
- Any abutment of any couple of cells should be free of DRC error.
- Wiring inside cell limited to Metal1 level.

Standard cell principles



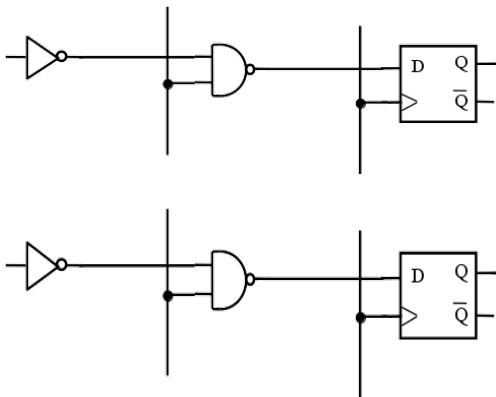
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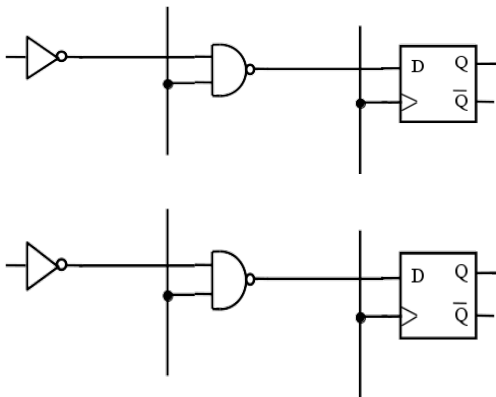
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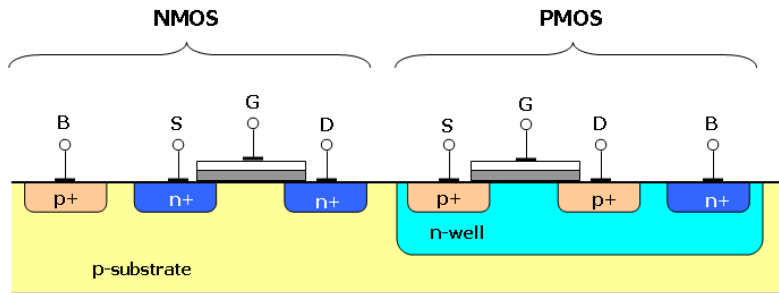
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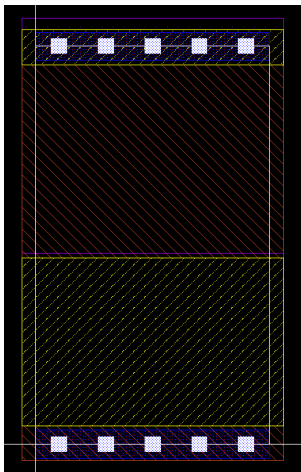
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Reference technology profile



gpdk045 standard cell template

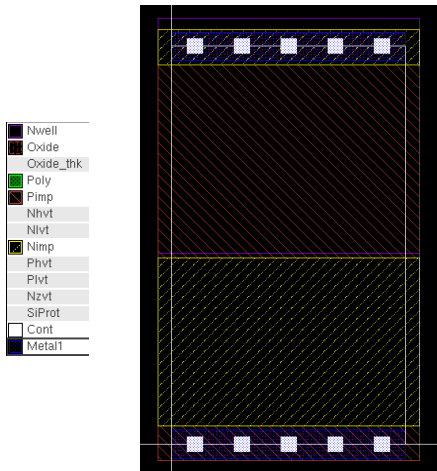
practical design



- NMOS areas and PMOS areas already filled.
- Body-ties areas for NMOS and PMOS already filled
- Body-ties already connected to V_{dd} (for PMOS) or V_{ss} (for NMOS)
- Simple abutment of cells fill an raw of cells with NMOS and PMOS areas.

gpdk045 standard cell template

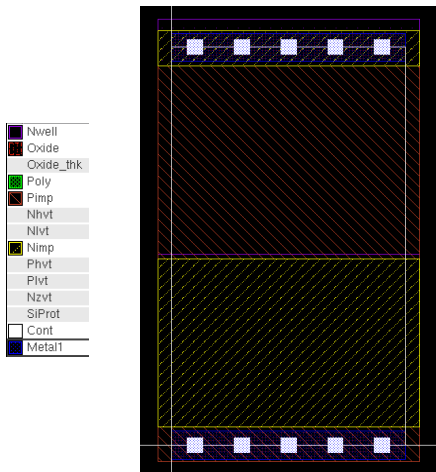
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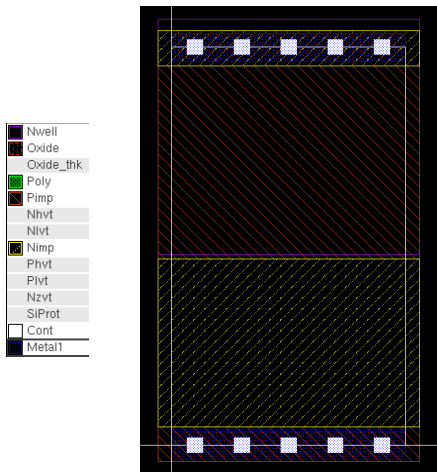
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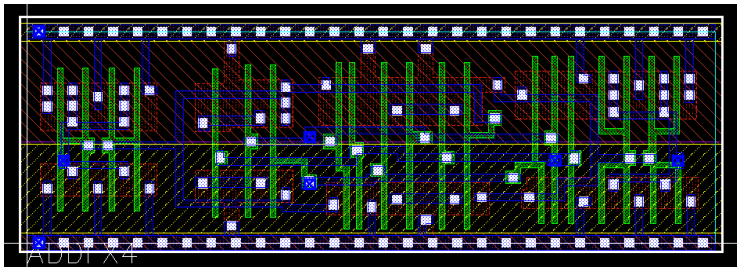


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gpdk045 adder

practical design















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	Oxide_thk
	Poly
	Pimpl
	Nhvt
	Nlvt
	Nimp
	Phvt
	Plvt
	Nzvt
	SiProt
	Cont
	Metal1

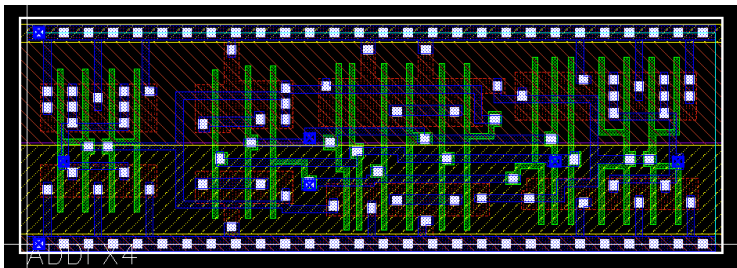


- All transistors have horizontal orientation.
- Maximal width defined by NMOS and PMOS areas height.
- Use parallel transistors for larger widths.
- Drain/Source implants may be used for local short wires (beware the resistivity).
- Global optimisation of Eulerian Paths (N(P)MOS subcircuits are graphs which visits every edge exactly once)

gpdk045 adder

practical design

	Nwell
	Oxide
	Oxide_thk
	Poly
	Pimp
	Nhvt
	Nlvt
	Nimp
	Phvt
	Plvt
	Nzvt
	SiProt
	Cont
	Metal1

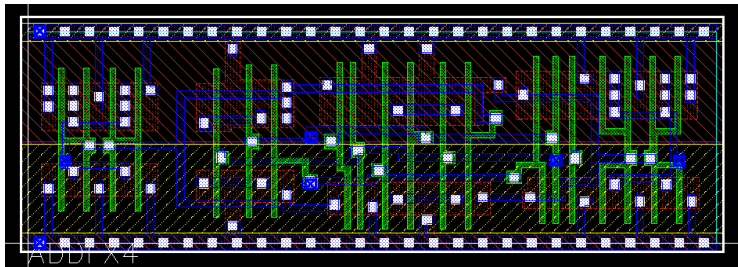


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	Cont
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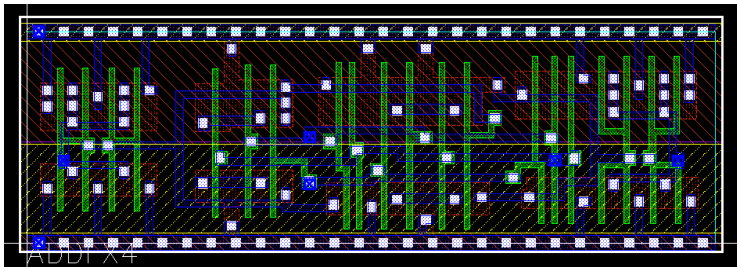


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practical design















	Nwell
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	Metal1

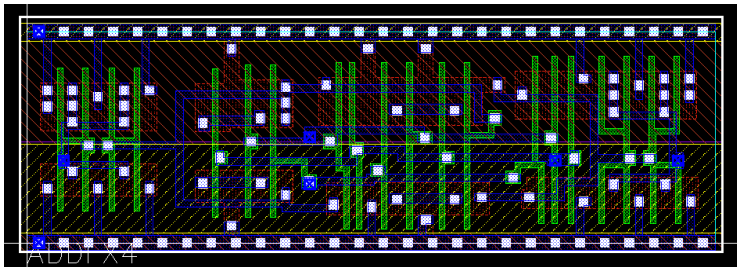


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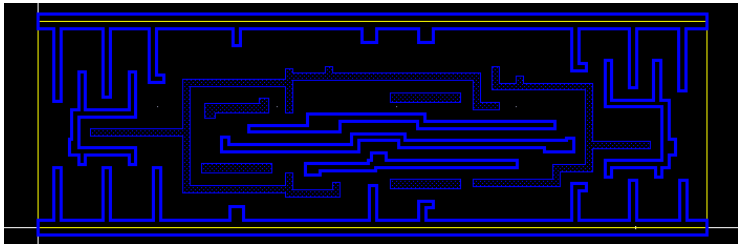


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gpdk045 adder abstract

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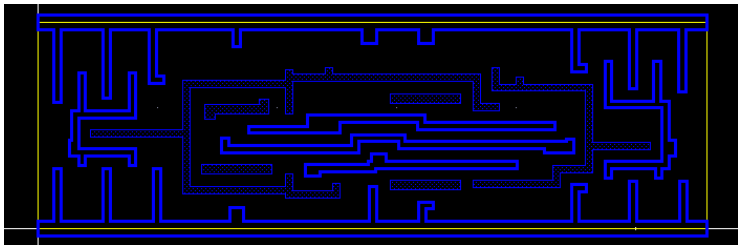


- Only needed informations for Place and Route.
- Wires connected to Input/Output pins of the cell
- Wires that are obstacles for wiring
- The router may use Metal1 has a wiring layer if enough room inside the cell

gpdk045 adder abstract

practical design















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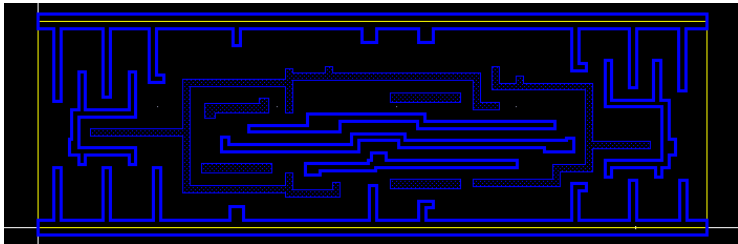


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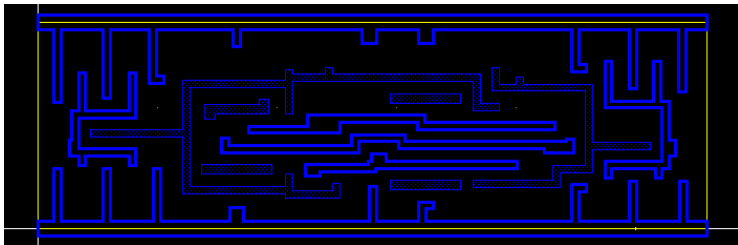


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Outline

Dynamic logic

Differential logic

Application specific logic

Performance optimization

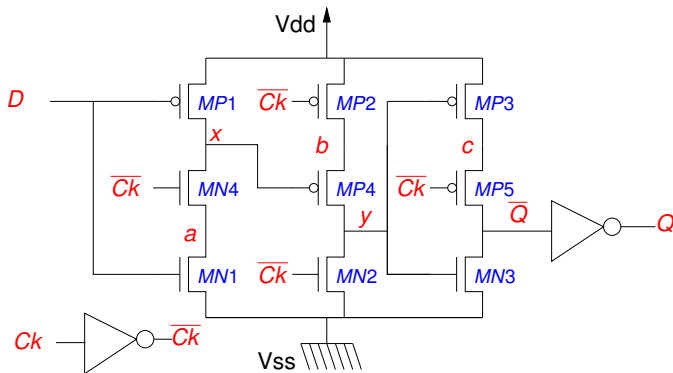
Sequential cells

Standard cell design

Practical work

Dynamic positive edge-triggered D flip-flop

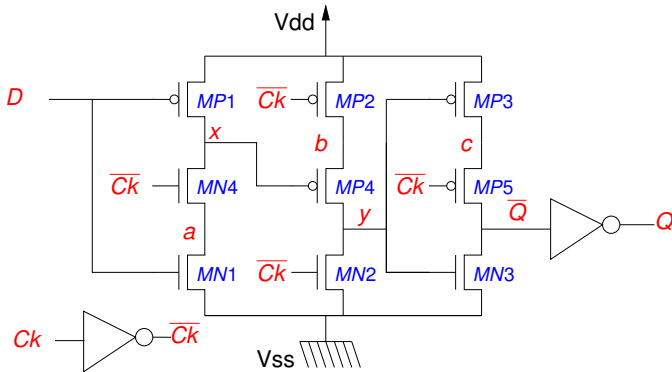
TSPC : True Single Phase Clock logic



- Very compact structure.
- Supposed to be faster than standard CMOS cell.

Dynamic positive edge-triggered D flip-flop

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Dynamic positive edge-triggered D flip-flop

Homework

- Question : How does this cell works ?
- Setup a table D, Q, Ck and all internal nodes of the cell.
- Add also the states of the MOS transistors (ON or OFF).
- Each internal node may have the states 0, 1, U(Unknown), Z0 (high-impedance 0), Z1 (high-impedance 1), or ZU (high-impedance Unknown).
- Imagine the following input sequence.



- Fill the table with the successive values of the signals
- Check if the cell is a D flip-flop.

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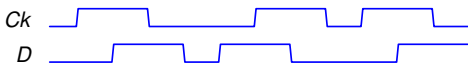


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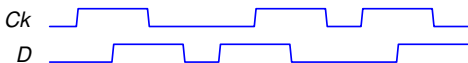


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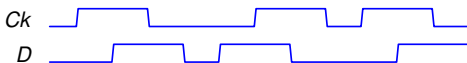


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